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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,196	05/20/2004	Fujio Ito	501.43736X00	7289

20457 7590 04/05/2005

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/849,196	ITO ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-8 drawn to a semiconductor device and the cancellation of claims 9-19 is acknowledged.

Claim Objections

2. Claims 3 and 7 recite the limitation "said first and second external terminals " in the claims. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Abe, US patent No. 6,410,979.

Regarding claim 1, Abe, teaches (fig. 2) a semiconductor device comprising: a semiconductor chip (14) having over a main surface thereof an integrated circuit and plural electrodes (upper surface of 14, col. 2, lines 54-60); plural leads (10) having end portions on one side fixed to a back surface of the semiconductor chip (14) and opposite end portions used as external terminals (10a); plural wires (16) for connecting the plural electrodes on the semiconductor chip with the plural leads positioned outside the semiconductor chip (refer to fig. 2); and a resin sealing member (18) for sealing the semiconductor chip (14), portions of the plural leads and the plural wires, the opposite end portions of the plural leads being exposed from a back surface of the resin sealing member (refer to fig. 2, where 10a is connected to 19).

Regarding claim 5, Abe, teaches (fig. 2) a semiconductor device comprising: an insulating base (12); a semiconductor chip having over a main surface thereof an integrated circuit and plural electrodes (upper surface of 14, col. 2, lines 54-60), the semiconductor chip being fixed over the insulating base (12); plural leads (10) end portions on one side of which are fixed to the insulating base and opposite end portions of which are used as external terminals (10a); plural wires (16) for connecting the plural electrodes formed on the semiconductor chip with the plural leads (10) positioned outside the insulating base (12); and a resin sealing member (18) for sealing the insulating base (12), the semiconductor chip (14), portions of the plural leads (10) and the plural wires (16), the opposite end portions of the leads being exposed from a back surface of the resin sealing member (refer to fig. 2, where 10a is connected to 19).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. Claims 2, 3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe in view of Minamio et al. US patent No. 6,642,609.

Regarding claims 2 and 6, Abe teaches substantially the entire claimed structure of claims 1 and 5 above except explicitly stating that the external terminals comprise first external terminals arranged along side faces of the resin sealing member and second external terminals arranged inside the first external terminals and each disposed between adjacent ones of the first external terminals.

Minamio teaches (figs. 4 and 5) an arrangement of external terminals (16) where first external terminals (terminals 16 that are arranged away from the face of the resin sealing 15) arranged along side faces of the resin sealing member (15) and second external terminals (terminals that are closer to the sealing member 15) arranged inside the first external terminals and each disposed between adjacent ones of the first external terminals (refer to fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arrangement of the first and second external terminals taught by Minamio in the structure of Abe in order to improve the package of the device.

Regarding claims 3 and 7, Abe teaches substantially the entire claimed structure of claims 1, 5, 2 and 6 above including the plural leads comprise plural first leads end portions on one side of which are positioned outside the semiconductor chip (the combined process of Abe and Minamio teaches leads that are away from the semiconductor device) and plural second leads each disposed between adjacent ones of the first leads and end portions on one side of which are fixed to the back surface of the semiconductor chip (refer to fig. 2 of Abe), wherein the plural first leads include first external terminals respectively (external terminals that are closer to the wall of the sealing member, fig. 4 of Minamio), and wherein the plural second leads include a second external terminals respectively (terminals that are away from the wall of the sealing member). The limitation of plural first leads end portions on one side of which are positioned outside the semiconductor chip does not preclude the semiconductor chip being on the plural first leads.

7. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe in view of Johnson US patent No. 5,726,079.

Regarding claims 4 and 8, Abe teaches substantially the entire claimed structure of claims 1 and 5 above except explicitly stating that a spacer fixed to an upper surface of the semiconductor chip and exposed partially from an upper surface of the resin sealing member.

Johnson teaches (fig. 1) the use of a spacer (heat sink 22) fixed to an upper surface of the semiconductor chip (12) and exposed partially from an upper surface of the resin-sealing member (26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the spacer structure taught by Johnson in the structure of Abe in order to improve heat dissipation property.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D and E are cited as being related to a packaging. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
April 1, 2005

EDDIE LEE
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